

FIG.1A

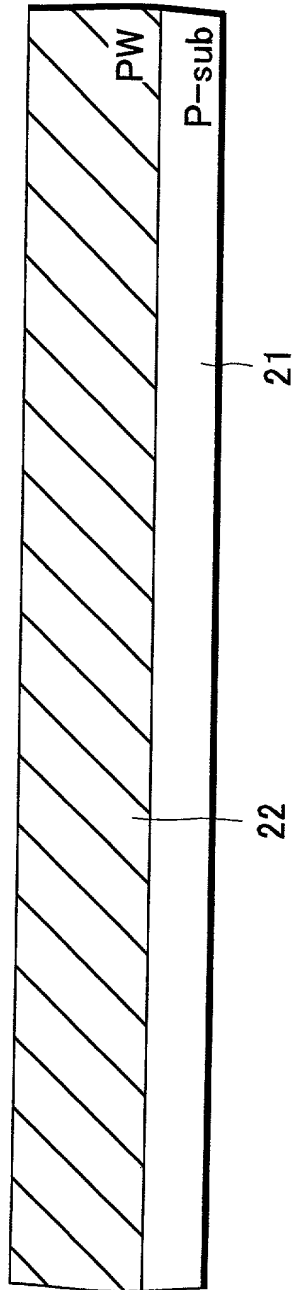
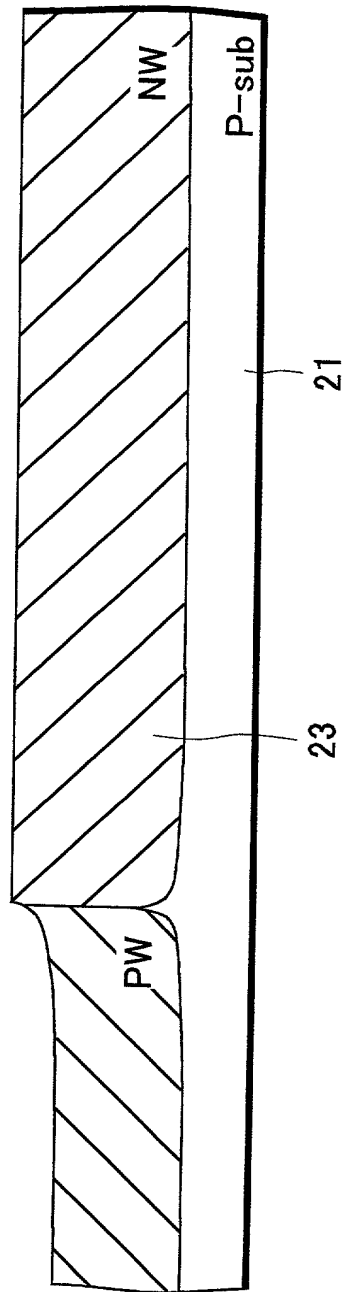


FIG.1B



This diagram shows a cross-sectional view of a semiconductor device. A P-substrate (P-sub) is at the base. Above it is a P-well (PW) region. A series of L-shaped structures (LN) are formed within the P-well, separated by regions labeled 24 and 25. A P-region (PR) is also indicated. The device is shown in a cross-section with a hatched pattern on the left side.

FIG.3A

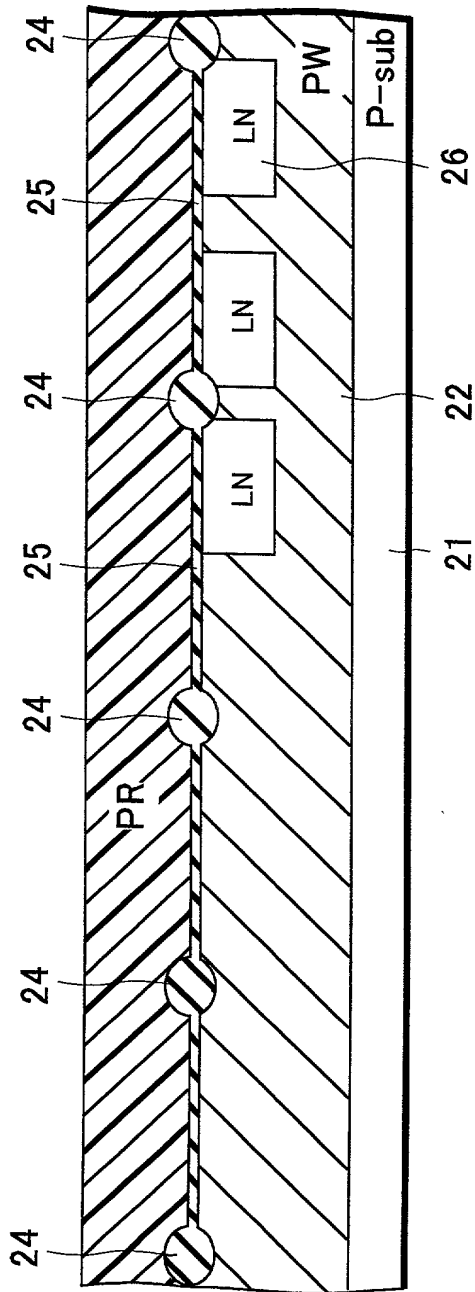


FIG.3B

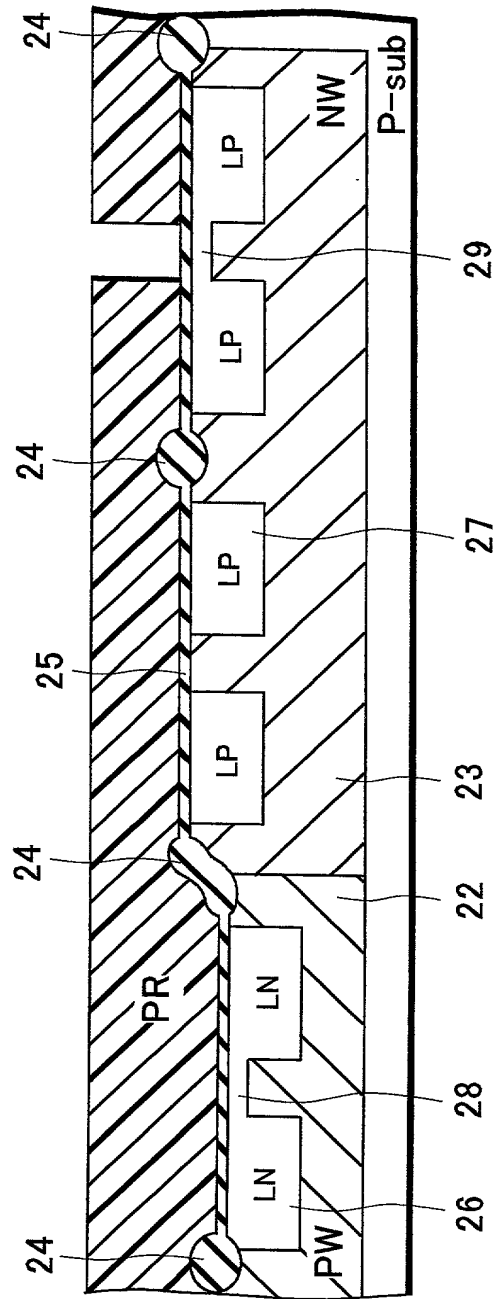


FIG.4A

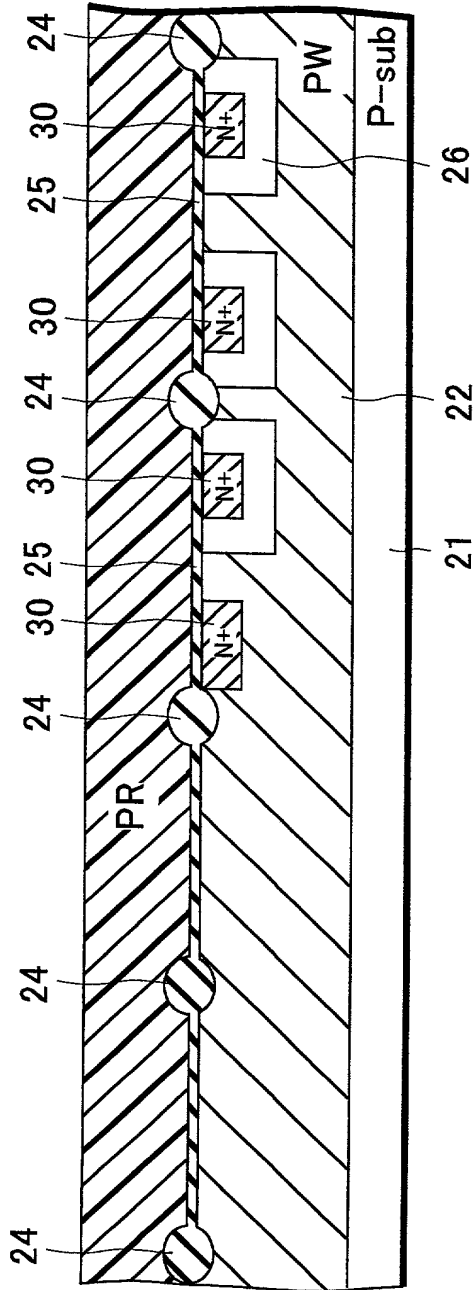


FIG.4B

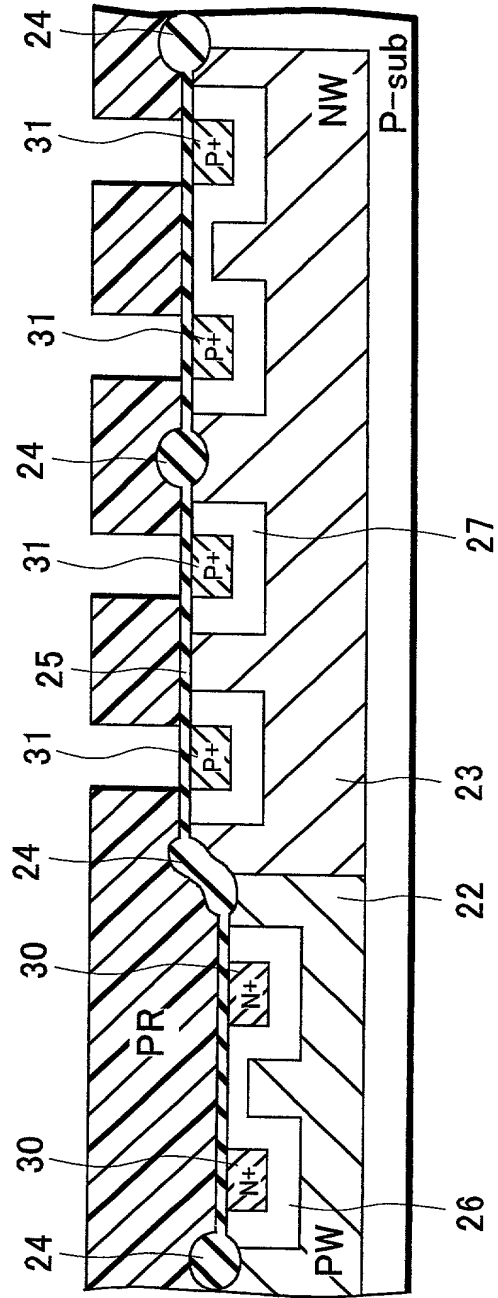


FIG.5A

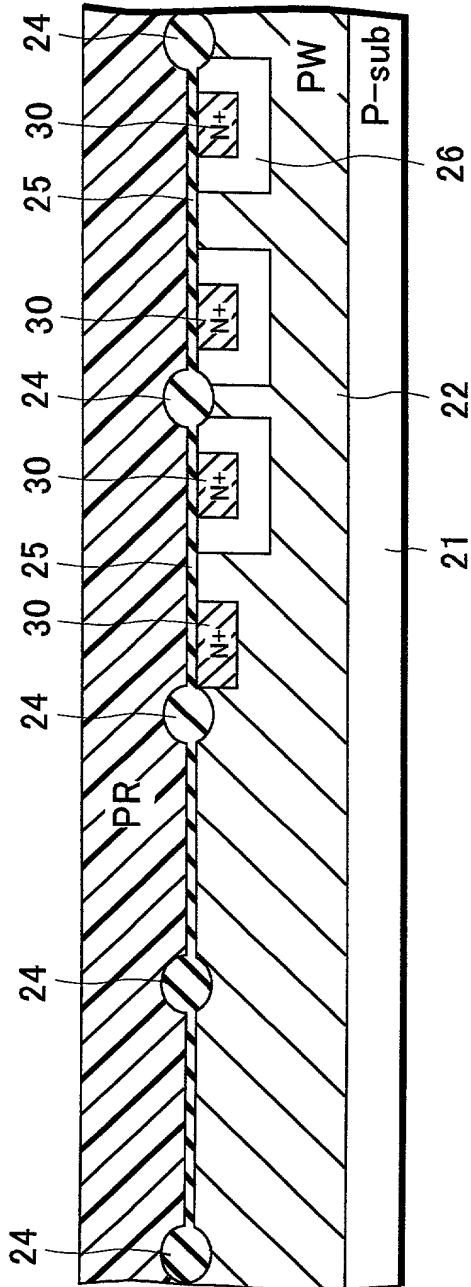
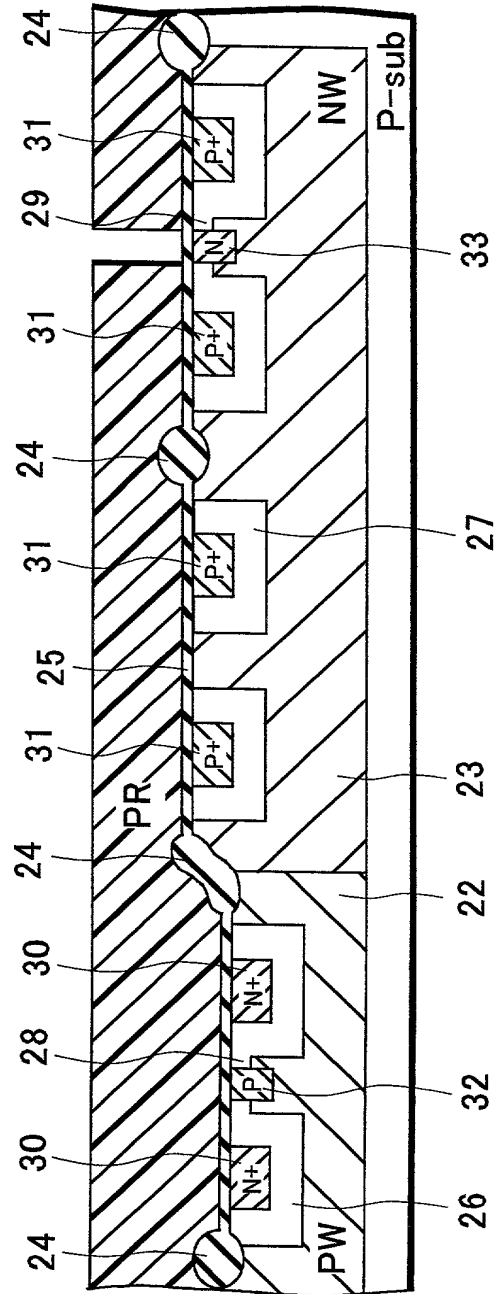


FIG.5B



This cross-sectional view shows a central channel (21) flanked by a source region (24) on the left and a drain region (24) on the right. The channel is defined by a central layer (26) and is surrounded by a gate stack (22). The gate stack consists of a gate dielectric (24) and a gate electrode (26). The source region (24) is formed by a source polysilicon layer (SPW) and a source nitride layer (SNW). The drain region (24) is formed by a drain polysilicon layer (PDW) and a drain nitride layer (DNW). The device is mounted on a substrate (34) with a passivation layer (35) on top.

[illegible]

FIG. 7A

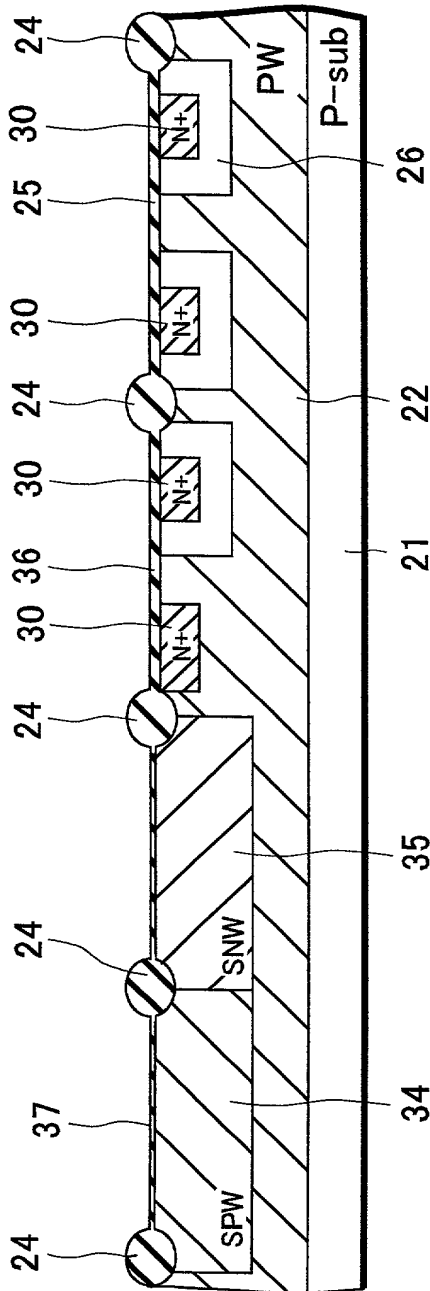


FIG. 7B

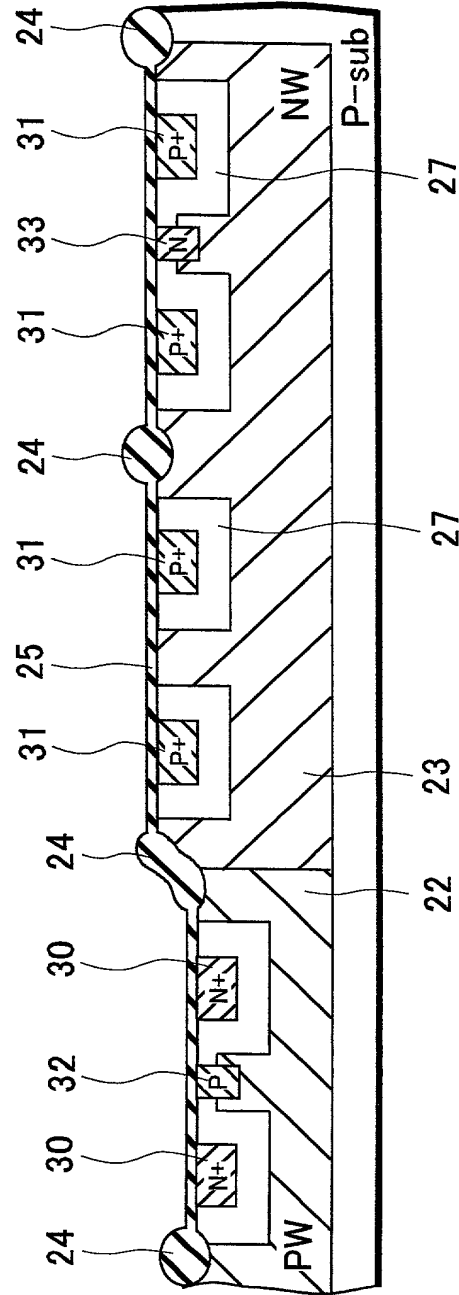


FIG.8A

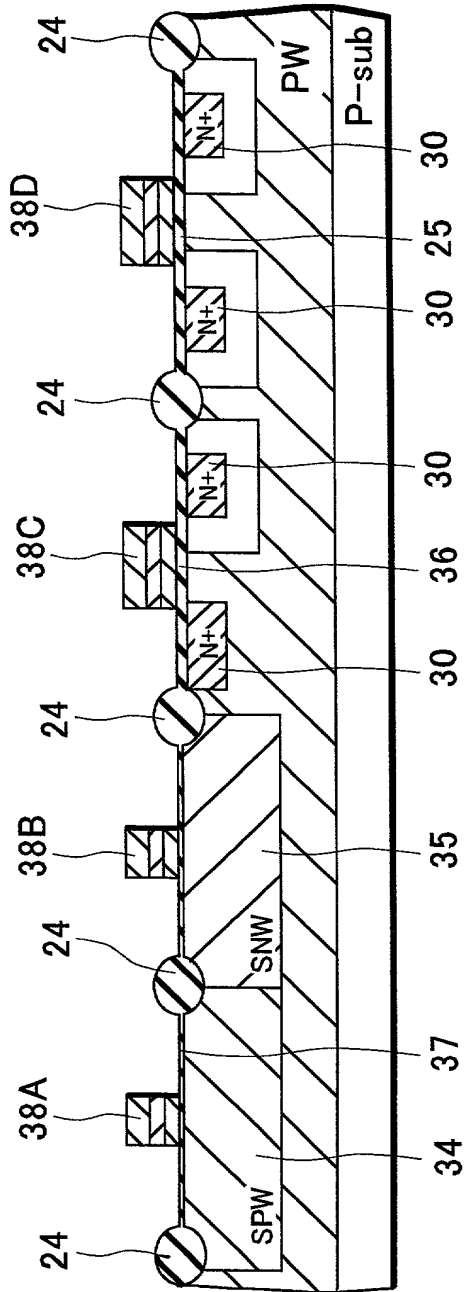
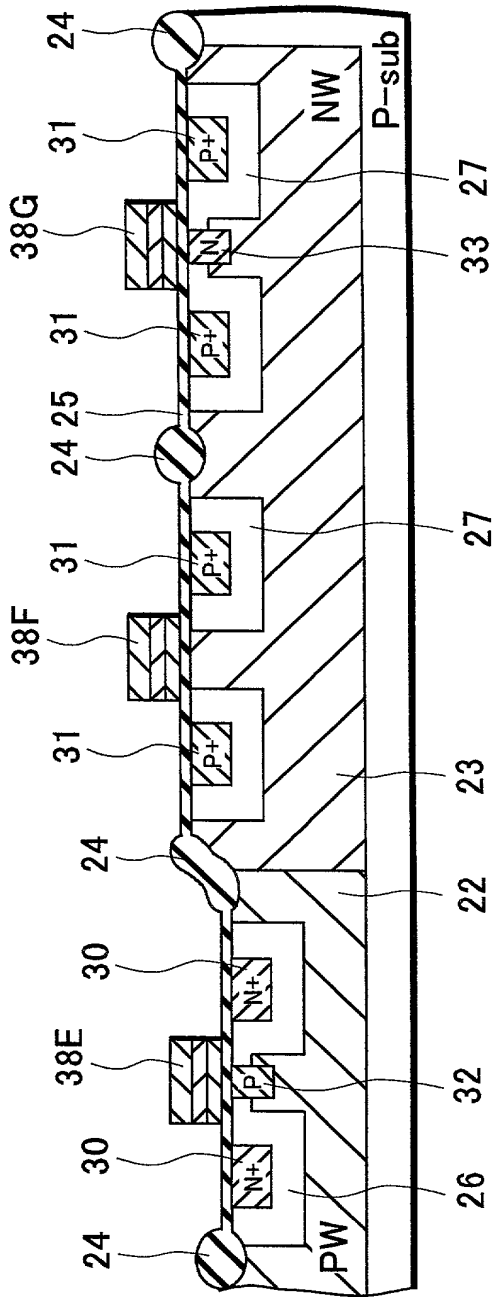


FIG.8B



This diagram shows a cross-sectional view of a semiconductor device. The structure is built on a P-substrate (P-sub). The device features several regions and layers: a top layer (24), a patterned layer (38A, 38B, 38C, 38D), a spacer layer (SPW, SNW), and a bottom layer (P-, N-, N+, PR, PW). The horizontal dimensions are indicated by arrows and labels: 24, 30, 25, 30, 30, 40, 40, 39, 39.

[illegible]

This cross-sectional view illustrates a semiconductor device with two rows of transistors. The left row features a source region (SPW) with an N+ layer, a gate stack (38A, 41A) on a P+ layer, a channel region (SNW) on an N+ layer, and a drain region (PR) with an N+ layer. The right row features a source region (PW) with an N+ layer, a gate stack (38B, 41B) on a P+ layer, a channel region (SNW) on an N+ layer, and a drain region (PR) with an N+ layer. The device is built on a P-substrate (P-sub). Various layers and contacts are labeled with reference numerals: 24 for the top surface, 38A and 38B for gate stacks, 41A and 41B for gate layers, 42 for source contacts, 43 for channel contacts, and 44 for drain contacts. The regions are labeled SPW, SNW, PR, PW, and P-sub.

This diagram shows a cross-sectional view of a semiconductor device. A central channel, labeled 24, is formed in a substrate, 26. The channel is defined by a series of gates, 27, which are formed on the top surface of the channel. The gates are labeled with various regions: 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41. The gates are formed by a series of layers: a bottom layer, 26, which is a p-type semiconductor; a middle layer, 27, which is a p-type semiconductor; and a top layer, 28, which is a p-type semiconductor. The gates are separated by spacers, 29, which are formed on the side walls of the channel. The spacers are labeled with various regions: 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41. The spacers are formed by a series of layers: a bottom layer, 26, which is a p-type semiconductor; a middle layer, 27, which is a p-type semiconductor; and a top layer, 28, which is a p-type semiconductor. The spacers are separated by gates, 27, which are formed on the top surface of the channel. The gates are labeled with various regions: 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41. The gates are formed by a series of layers: a bottom layer, 26, which is a p-type semiconductor; a middle layer, 27, which is a p-type semiconductor; and a top layer, 28, which is a p-type semiconductor.

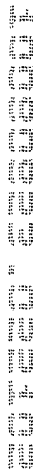
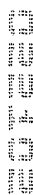
[illegible][illegible]

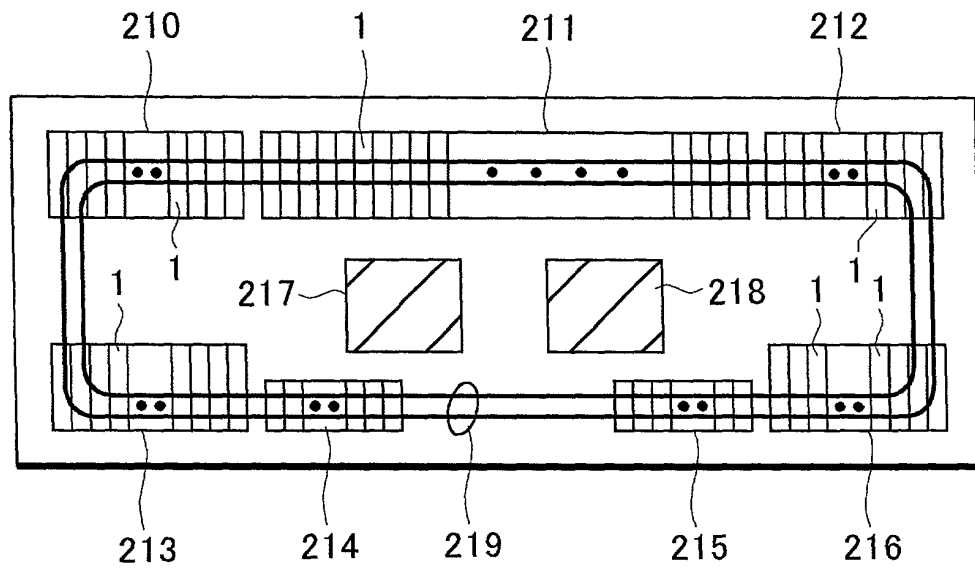
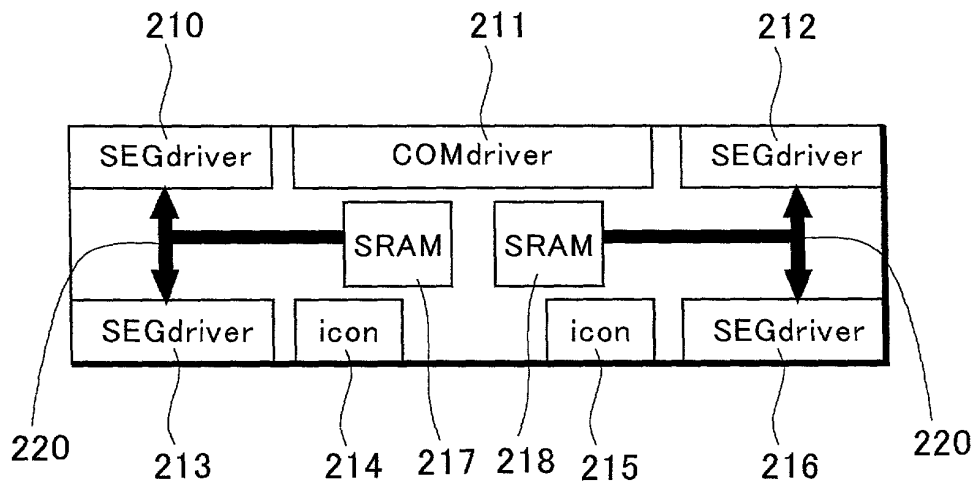
FIG. 12**FIG. 13**

FIG. 14A

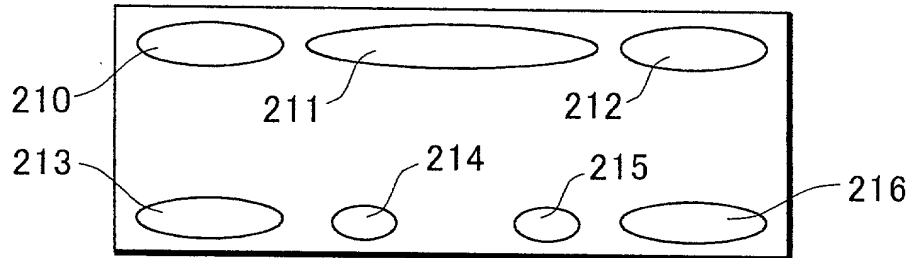


FIG. 14B

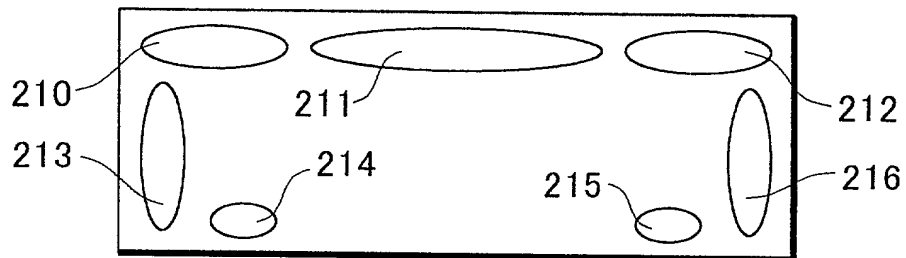


FIG. 14C

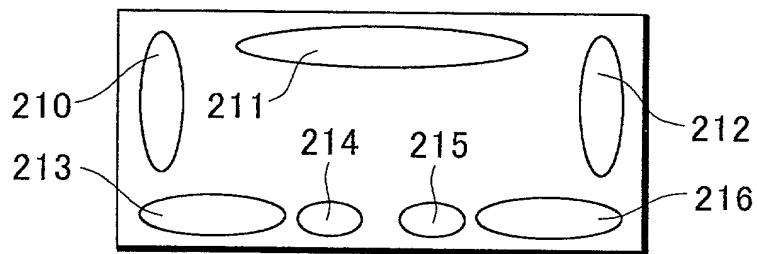


FIG. 14D

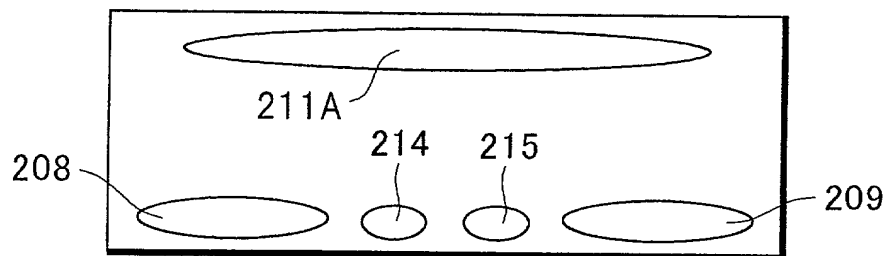


FIG. 15

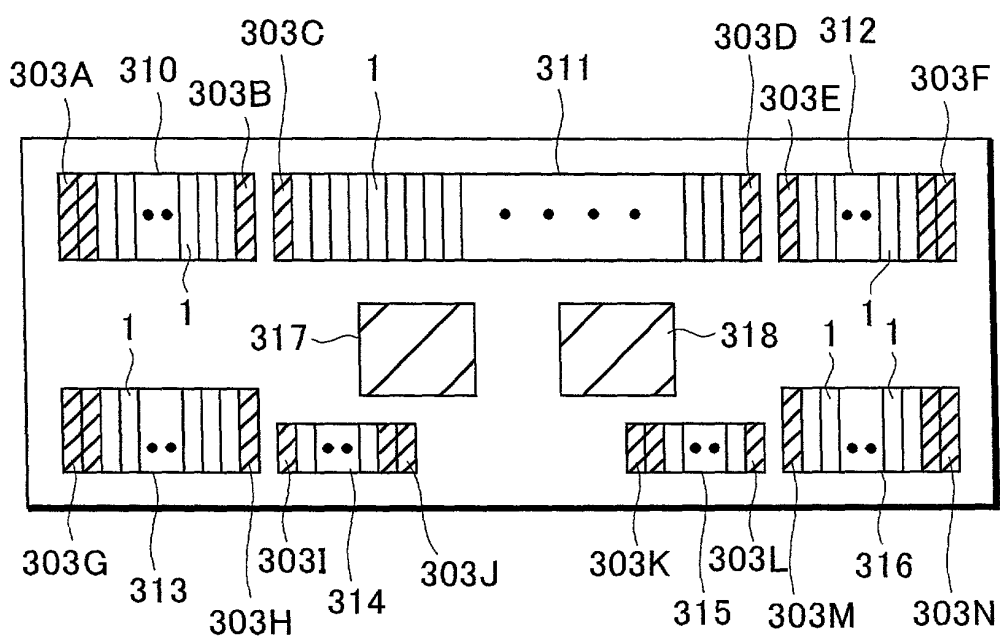


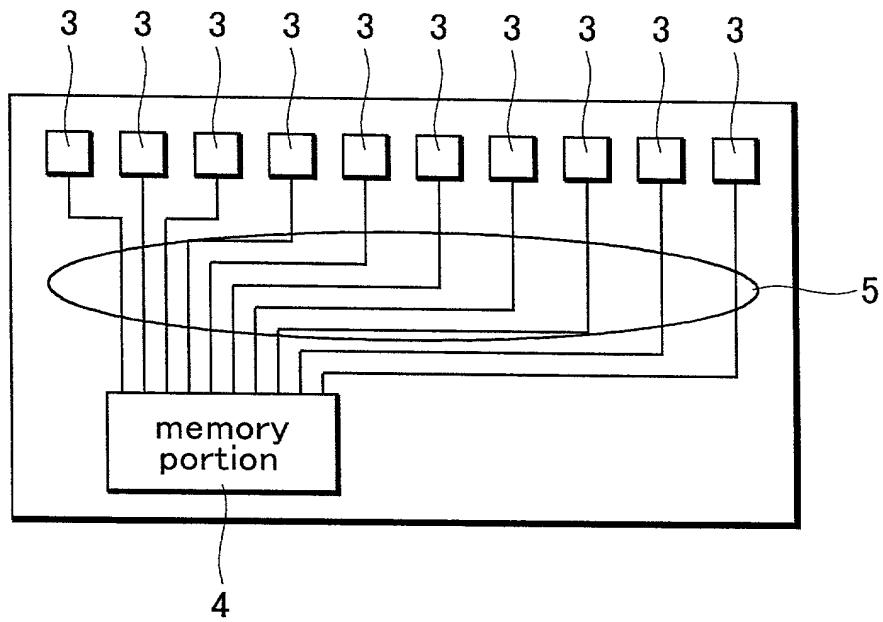
FIG. 16

FIG.17A

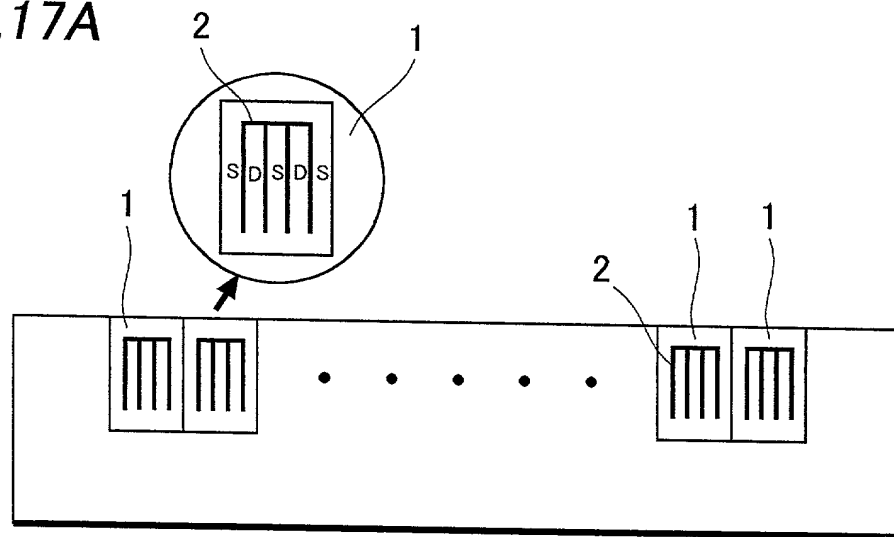


FIG.17B

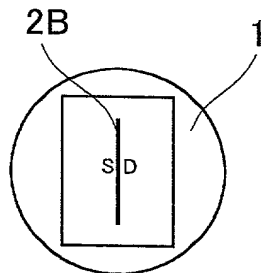


FIG.17C

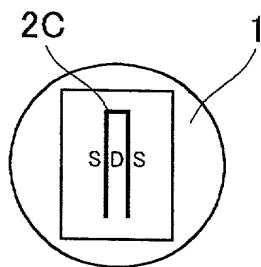


FIG.17D

